IN THE CLAIMS

1 – 9. (canceled).

10. (currently amended) ~~The integrated circuit chip package of claim 9~~An integrated circuit chip package comprising:

a metal substrate core;

the metal substrate core having at least two electrically isolated regions;

wherein at least one of the electrically isolated regions of the metal substrate core is coupled with a digital ground of an integrated circuit chip, wherein input and output signals of the integrated circuit chip are routed through the electrically isolated region of the metal substrate core that is coupled with the digital ground of the integrated circuit chip, and wherein at least one ~~other~~ of the electrically isolated regions of the metal substrate core is coupled with an operating voltage rail of the integrated circuit chip.

11. (currently amended) The integrated circuit chip package of claim ~~9~~ 10, wherein at least one ~~other~~ of the electrically isolated regions of the metal substrate core is coupled with an analog ground of the integrated circuit chip

12. (canceled)

13. (currently amended) ~~The integrated circuit chip package of claim 12~~ An integrated circuit chip package comprising:

a metal substrate core;

the metal substrate core having at least three electrically isolated regions;

wherein at least one of the electrically isolated regions of the metal substrate core is coupled with a digital ground of an integrated circuit chip and through this region input and output signals are routed, and wherein at least one ~~other~~ of the electrically isolated regions of the metal substrate core is coupled with an operating voltage rail of the integrated circuit chip.

14. (currently amended) The integrated circuit chip package of claim ~~12~~ 13, wherein at least one ~~other~~ of the electrically isolated regions of the metal substrate core is coupled with an analog ground of the integrated circuit chip.

15 – 20. (canceled).